

UART

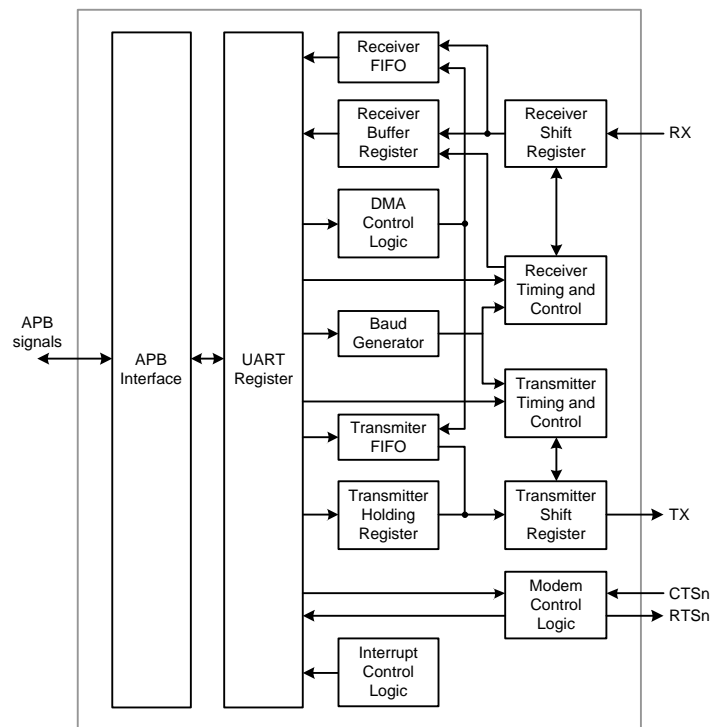
Universal Asynchronous Receiver/Transmitter (UART) Intellectual Property (IP).

Description

It performs serial-to-parallel conversion on data originating from other serial devices, and performs parallel-to-serial conversion on data from a CPU to these devices. Asynchronous serial data communication are synched by start-stop in character units and can communicate with a universal asynchronous receiver/transmitter(UART)

Features

- baud rate generator with programmable bit rates.
- 16/32/64/128-Byte FIFOs Reduce CPU Interrupts
- Full duplex communication:
The transmitting and receiving sections are independent, so the UART can transmit and receive simultaneously.
- UART are selectable serial data communication formats.
 - Data length : seven or eight bits
 - Stop bit length : one or two bits
 - Parity : even, odd or no-parity bit generation and detection.
 - Receive error detection : parity, overrun, and framing errors
- Two types of interrupts:
 - Transmit-data-empty, Receive-data-full are requested independently.
- Optional AHB,APB and custom bus interfaces



Application Area : Serial Computer Interface, Serial interface other devices.

Available Documents : Data Sheet

Design File Formats : EDIF File Format , VHDL/Verilog Code

Verification : Verilog Testbench

Simulation Tool Used : Model Technology ModelSim™ 6.4