SCI

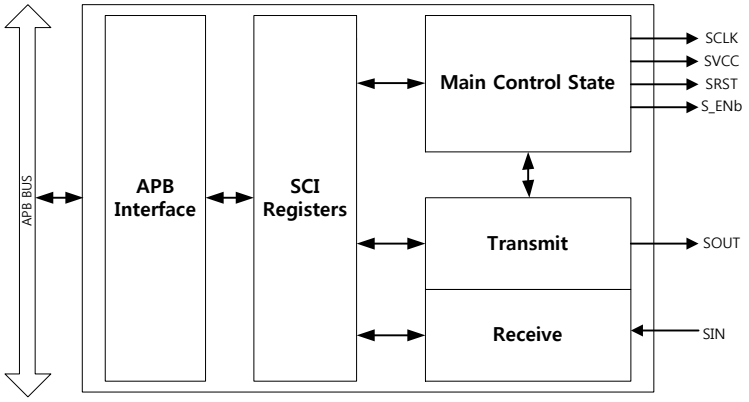
Smart Card Interface (SCI) Intellectual Property (IP).

Description

The SCI support ISO7816-3 Asynchronous T=0 and T=1 Standard Protocol. The SCI autonomously control data transfer to and from the smart card reader . Transmit and Receive data are provided to reduce the required interaction between the host CPU and the peripheral.

Features

- TxFIFOs/RxFIFOs Reduce CPU Interrupts
- Support Asynchronous T0 and T1 transmission Protocols
- Support clock rate conversion factor
- Hardware Initiated Card Deactivation sequence on detection of card removal
- Software Initiated Card Activation and Card Deactivation sequence on transaction
- Parity bit generation and detection and Auto retransmission
- Automatic direct and inverse convention detection
- Check for ISO7816-3 Operation Status
  - De-bounce check for Smart Card Insertion
  - First Character(TS) not receive within 40000 smart card clock
  - ATR data stream exceeded the specified time
  - Maximum Character interval between the leading edges of the start bits of two consecutive characters
  - Maximum Block interval between the leading edges of the start bits of two consecutive characters sent in opposite direction
  - Transmit buffer empty / Receive buffer full
  - Parity error count / De-activation complete
- Optional AHB,APB and custom bus interfaces



Application Area : Smart Card interface, smart card dummy terminal, EFT-POS, PIN-PAD

Available Documents : Data Sheet

Design File Formats : EDIF File Format , VHDL/Verilog Code

Verification : Verilog Testbench

Simulation Tool Used **:** Model Technology ModelSim™ 6.4